

YIELD IMPROVEMENT THROUGH PROBE-BASED CACHE SIZE REDUCTION

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ABSTRACT OF DISCLOSURE

10 A multiple-way cache memory having a plurality of cache
blocks and associated tag arrays includes a select circuit
that stores way select values for each cache block. The way
select values selectively disable one or more cache blocks
from participating in cache operations by forcing tag
comparisons associated with the disabled cache blocks to a
mismatch condition so that the disabled cache blocks will not
15 be selected to provide output data. The remaining enabled
cache blocks may be operated as a less-associative cache
memory without requiring cache addressing modifications.

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